

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : John M. RUDOSKY et al. Art Unit : Unknown
Serial No. : Unknown Examiner : Unknown
Filed : Herewith
Title : VITERBI DECODER WITH SURVIVOR BITS STORED TO SUPPORT LOOK-
AHEAD ADDRESSING

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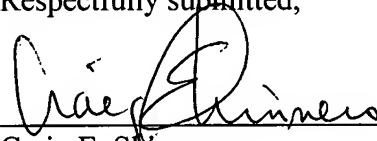
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Respectfully submitted,

Date: Feb. 18, 2004



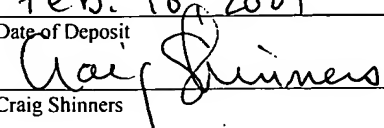
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	Unknown
				Filing Date	Herewith
				First Named Inventor	John M. RUDOSKY
				Group Art Unit	Unknown
				Examiner Name	Unknown
Sheet	2	of	2	Attorney Docket Number	021202-100100US

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	C1	George C. Clark, Jr., and J. Bibb Cain, Error Correction Coding for Digital Communications, Plenum Press, New York, 1981.	
	C2	Hekstra, Andries P., "An Alternative to Metric Rescaling in Viterbi Decoders", IEEE Transactions on Communications, Vol. 37, No. 11, Nov 1989.	
	C3	E. Yeo, S. Augsburger, W. R. Davis, and B. Nikolic, "Implementation of High Throughput Soft Output Viterbi Decoders," Proc. IEEE Workshop on Signal Processing Systems, , pp. 146-151, San Diego, CA, Oct 16-18, 2002.	
	C4	M. Bickerstaff, et al., "A Unified Turbo/Viterbi Channel Decoder for 3GPP Mobile Wireless in 0.18µm CMOS", in IEEE Journal of Solid-state Circuits, Vol. 37, No. 11, November 2002 pg. 1555-1562	
	C5	A. Matache, R. D. Wesel, Jun Shi, "Trellis Coding for Diagonally Layered Space-Time Systems".	
	C6	D. Garrett, M. Stan, "Low Power Architecture of the Soft-Output Viterbi Algorithm".	
	C7	Jong Min Kim, Nan Jin Park, "Implementation of Convolutional Encoder and Viterbi Decoder for Wideband CDMA PCS Baseband Processing Unit Using Multiple TMS320C40s".	
	C8	I. Bogdan, M. Munteanu, P.A. Ivey, N. L. Seed, N. Powell, "Power Reduction Techniques for a Viterbi Decoder Implementation".	
	C9	E. Paaske, J. D. Andersen, "High Speed Viterbi Decoder Architecture", First ESA Workshop on Tracking, Telemetry and Command Systems, ESTEC, June 1998.	
	C10	Yun-Nan Chang, Keshab K. Parhi, Hiroshi Suzuki, " Low-power Bit-serial Viterbi Decoder for Next Generation Wide-band CDMA Systems".	
	C11	H. Hendrix, "Viterbi Decoding Techniques in the TMS320C54x Family", Texas Instruments Application Note, June 1996.	

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